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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,568	01/22/2002	Mou-Shiung Lin	JCLA8533	6093

23900 7590 02/17/2005

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/055,568	Applicant(s) LIN ET AL.	
	Examiner James M. Mitchell	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 143-167 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 143-167 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This office action is in response to the request for continued examination filed November 8, 2004.

Specification

Claims 158 and 159 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s). The added limitation that the die is positioned in an opening of a silicon layer above a heat-conducting layer is mutually exclusive from the die being mounted on the silicon substrate. The claim has not been furthered examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 164 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear how the word "bulk" further limits silicon.

Claim Rejections - 35 USC § 102

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 143-145, 148-151, 156, 157, 160-162, 164-167 are rejected under 35 U.S.C. 102(e) as being anticipated by Maruyama (U.S. 2001/0042901).

Maruyama (Fig 17A-D) discloses (cl.143, 164, 165) a substrate comprising bulk silicon (i.e. understood to mean only a silicon material; par. 0083), only one die (12) mounted to said substrate, said die having an active surface (Par. 0083; in contact with item 13; Fig 20), internal circuitry and a plurality of active devices (Par. 0126), said active surface including multiple pads (13) electrically connected to said active devices through said internal circuitry (21), said substrate having a surface not covered by said die, and at least one patterned line (15) extending over said active surface of said die and over a surface of the substrate (Fig 20; portion of line extends over area of substrate not covered by die), said patterned line connected to one of pads (e.g. Fig 2, item 13), said line is a conductive material that can form part of a circuit and therefore is a circuit layer; (cl. 144, 166, 167) with the distance of item 15 (Fig 17C) from side to side a thickness/ width greater than the distance of item 21 and therefore its width; (cl. 148-151) and a dielectric layer (19,22) positioned over said active

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surface and over the patterned line that has pores (i.e. all material has a degree of porosity, including holes created by vias ,21 & 16; (cl.156, 157) with the die is in a cavity (i.e. region taken by item 12) and in the same plane as the substrate and is therefore coplanar; (cl. 159, 162) further that the insulating material is a polymer consisting of epoxy (Par. 0174); (cl. 160, 161) and said die side surfaces (i.e. each surface of the die is a side surface) is enclosed by said polymer and coplanar (i.e. horizontal plane passes through item 22 and the item 12).

Claims 143 and 163 are rejected under 35 U.S.C. 102(e) as being anticipated by Hozoji et al. (U.S. 2002/0079575).

Hozoji (Fig 7) discloses (cl. 143) discloses a substrate comprising bulk silicon (i.e. understood to mean only a silicon material; 2), only one die (1) mounted to said substrate, said die having an active surface (i.e. lower portion of flip-chip), internal circuitry and a plurality of active devices (i.e. "device"), said active surface including multiple pads (6) electrically connected to said active devices through said internal circuitry, said substrate having a surface not covered by said die, and at least one patterned line (3) extending over said active surface of said die and over a surface of the substrate, said patterned line connected to one of pads (8), said line is a conductive material that can form part of a circuit and therefore is a circuit layer; (cl. 163) and further comprising multiple solder balls (5).

Claim Rejections - 35 USC § 103

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 146-147 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (U.S 2001/0042901) as applied to claim 143 and further in combination with Gonzalez (U.S. 2003/0080437)).

Maruyama does not appear to show a ground or bus positioned above the active components.

Gonzalez (Par. 0004, 0024) teaches forming passive components such as capacitors, resistors and inductors on a substrate and connecting them to a chip/die.

It would have been obvious to one of ordinary skill in the art to incorporate either a bus and ground above the active components of Murayama in order to provide a shielding and to couple various components as is taught in Gonzalez (Par. 0024)

Claims 152-155 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (U.S 2001/0042901) as applied to claim 143 and further in combination with Sakaf et al. (U.S. 2001/0033474).

Maruyama does not appear to show forming passive components such as capacitors, resistors and inductors on a substrate and connecting them to a chip/die.

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Sakaf (Par. 007) teaches forming passive components such as capacitors, resistors and inductors on a substrate and connecting them to a chip/die.

It would have been obvious to one of ordinary skill in the art to incorporate forming a passive component on the substrate of Murayama in order to provide a component for use in mobile communication terminal devices.

CA
2/15/2005

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2808

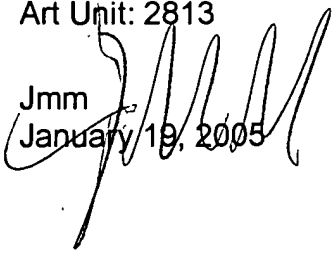
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Jmm

January 19, 2005

A large, stylized handwritten signature in black ink, appearing to be 'Jmm', is written over the text 'Jmm' and 'January 19, 2005'.